Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A MOS (metal on semiconductor transistor) structure for ESD protection, comprising:

an active region, defined on a substrate of a second-type conductivity;

a channel region separating the active region into a first drain/source region and a second drain/source region;

at least one first island, formed on the first drain/source region and having a first conductive segment and a first gate oxide segment of the first thickness, the first conductive segment being stacked on the first gate oxide segment;

a doped drain region of a first-type conductivity in the first drain/source region, defined substantially by a field oxide region, the channel region and the at least one first island; and

a breakdown-enhanced layer, formed in the first drain/source region and contacting the doped drain region, to reduce a breakdown voltage across the doped drain region and the substrate.

2. (Original) The MOS structure as claimed in claim 1, wherein the MOS structure has, within the active region, two breakdown-enhanced layers with the same depth and the same dosage, and one of the breakdown-enhanced layers is inside the first drain/source region while another is outside the

first drain/source region.

3. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer has the first-type conductivity.

4. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer also forms pocket-implanted structures of internal MOS.

5. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer has the second-type conductivity.

6. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer also forms anti-punch-through structures of internal MOS.

7. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer is formed under the doped drain region.

8. (Original) The MOS structure as claimed in claim 1, wherein the channel region has a gate structure consisting of a second conductive segment and a second gate oxide segment, the second conductive segment being stacked on the second gate oxide segment.

9. (Original) The MOS structure as claimed in claim 8, wherein the second gate oxide and the first gate oxide have the same thickness.

10. (Original) The MOS structure as claimed in claim 8, wherein the second gate oxide and the first gate oxide have different thicknesses.

11. (Original) The MOS structure as claimed in claim 10, wherein the second gate oxide is thicker than the first gate oxide.

12. (Currently Amended) The MOS structure as claimed in claim 11, wherein the breakdown-enhanced layer is formed [[at]] near the at least one first island ~~breakdown enhanced layer~~ and in an internal-circuit MOS transistor with the first gate oxide thickness simultaneously.

13. (Original) The MOS structure as claimed in claim 1, wherein the breakdown-enhanced layer is not formed in the second drain/source region.

14. (Original) The MOS structure as claimed in claim 1, wherein the channel region has a field oxide stacked on the substrate.

15. (Withdrawn) An electrostatic discharge protection device on a substrate of a second-type conductivity, comprising:

a source region of a first-type conductivity, coupled to a power rail;

a drain region of the first-type conductivity, coupled to a pad via a contact;

a first gate structure placed between the source region and the drain region, for controlling electric connection between the drain region and the source region; and

a second gate structure substantially surrounded by the drain region, for distancing the contact from the first gate structure;

wherein the first gate structure and the second gate structure receives different implant treatments.

16. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein the second gate structure distances the contact from the first gate structure.

17. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein the first gate structure includes an adjacent first doped junction; the second gate structure includes an adjacent second doped junction; and the first and second doped junctions have different doping profiles.

18. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein a gate oxide of the first gate structure and a gate oxide of the second gate structure have the same thickness.

19. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein a gate oxide of the first gate structure and a gate oxide of the second gate structure have different thicknesses.

20. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein the gate oxide of the first gate structure is thicker than the gate oxide of the second gate structure.

21. (Withdrawn) The electrostatic discharge protection device as claimed in claim 15, wherein the second gate structure receives breakdown-

enhanced implantation while the first gate structure is sheltered from the breakdown-enhanced implantation.

22. (Withdrawn) The electrostatic discharge protection device as claimed in claim 21, wherein the breakdown-enhanced implantation is pocket implantation to form pocket-implanted structures.

23. (Withdrawn) The electrostatic discharge protection device as claimed in claim 21, wherein the breakdown-enhanced implantation is anti-punch-through implantation.

24. (Withdrawn) The electrostatic discharge protection device as claimed in claim 21, wherein the breakdown-enhanced implantation is to form a breakdown-enhanced layer under the drain region.

25. (Withdrawn) The electrostatic discharge protection device as claimed in claim 24, wherein the breakdown-enhanced layer has the second-type conductivity.

26. (Withdrawn) An electrostatic discharge protection device, comprising:

an active region on a substrate of a second-type conductivity;

a first gate structure and a second gate structure, both being placed on the active region;

at least one drain region of a first-type conductivity and one source region of the first-type conductivity, defined and separated by either the first gate structure or the second gate structure; and

a breakdown-enhanced layer, formed within the drain region to reduce a breakdown voltage across the drain region and the substrate.

27. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the at least one drain region and one source region are respectively coupled to a pad and a power rail.

28. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the breakdown-enhanced layer is not present within the source region

29. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein a gate oxide of the first gate structure is thicker than a gate oxide of the second gate structure.

30. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the first gate structure separates the active region into two drain/source regions as well as the second gate structure does.

31. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the breakdown-enhanced layer has the first-type conductivity.

32. (Withdrawn) The electrostatic discharge protection device as claimed in claim 31, wherein the breakdown-enhanced layer also forms pocket-implanted structures of internal MOS.

33. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the breakdown-enhanced layer has the second-type conductivity.

34. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the breakdown-enhanced layer also forms anti-punch-through structures of internal MOS.

35. (Withdrawn) The electrostatic discharge protection device as claimed in claim 26, wherein the breakdown-enhanced layer is formed under the doped drain region.

36. (New) A first MOS (metal on semiconductor) structure for ESD protection, comprising:

an active region defined on a substrate of a second-type conductivity;

a channel region separating the active region into a first drain/source region and a second drain/source region;

the first drain/source region including a first doped region;

at least one distributed junctions formed within the first drain/source region and completely surrounded by the first doped region;

the at least one distributed junctions including a first junction being spaced apart from the channel region; and

a breakdown-enhanced layer formed at an edge of the first junction.

37. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer has a first-type conductivity.

38. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer includes a pocket-implant.

39. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer has the second-type conductivity.

40. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer includes an anti-punch-through implant.

41. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer is formed under the doped drain region.

42. (New) The structure as claimed in claim 36, wherein the breakdown-enhanced layer is not formed in the second drain/source region.

43. (New) The structure as claimed in claim 36, wherein the channel region has a field oxide stacked on the substrate.

44. (New) The structure as claimed in claim 36, wherein the first doped region comprises heavily doped ions and the first junction encloses a first sub-region substantially without the heavily doped ions.

45. (New) The structure as claimed in claim 44, wherein a first oxide segment overlying said first sub-region and a first conductive segment stacked on the first oxide segment over the first sub-region.

46. (New) The structure as claimed in claim 45, wherein the channel region has a gate structure consisting of a second conductive segment and a second gate oxide segment, the second conductive segment being stacked on the second gate segment.

47. (New) The structure as claimed in claim 46, wherein the second gate oxide segment and the first gate oxide have the same thickness.

48. (New) The structure as claimed in claim 46, wherein the second gate oxide and the first gate oxide have different thickness.

49. (New) The structure as claimed in claim 46, wherein the second gate oxide is thicker than the first gate oxide.